ECE 2250 - Final Report

SIDO Buck Converter Analysis & Testing

Group 7

Fall 2023

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I Abstract

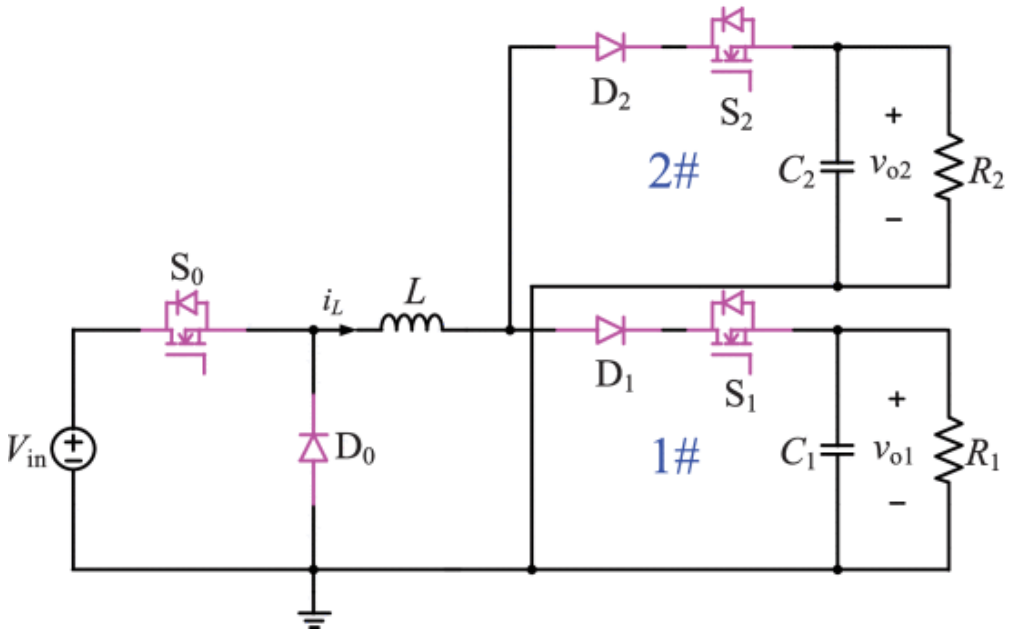
As opposed to the traditional single-input single-output (SISO) DC-DC converter topologies, single-input dual-output (SIDO) DC-DC converters provide the advantage of being able to provide 2 power outputs from one input. However, SIDO topologies present challenges during modeling and implementation, specifically the highly nonlinear nature of the circuit and the complex control scheme used. In this paper, we build upon the results of "Multiple-Harmonic Modeling and Analysis of Single-Inductor Dual-Output Buck DC–DC Converters" [1] by verifying the mathematical analysis, introducing new simulation results, and introducing new results of testing a practical implementation.

II Overview & Goals

Multiple-output DC-DC converter technology is gaining popularity in applications requiring multiple regulated DC output terminals. For example, electric vehicle power distribution networks and telecommunication networks require precisely regulated DC sources of multiple outputs, often from a single source [2].

These multiple-output systems introduce more complex topologies that introduce novel challenges in the design and implementation of such systems. Specifically, multi-stage control systems and highly non-linear characteristics arise.

The converter analyzed in this paper consists of a buck converter covered in class with a MOSFET-multiplexed output stage, as seen in the figure below. This topology was suggested and analyzed by [1].



SIDO Buck Converter Topology in Question

S_1 and S_2 are tied together in a complementary fashion - i.e., when S_1 is on, S_2 is off, and vice versa. R_1 and R_2 represent 2 separate loads. S_0 operates on a separate control scheme from S_1 and S_2.

The goals of this paper are twofold:

1. Use a novel approach to modeling & simulation of the circuit and control system to verify the results of [1].

2. Implement the SIDO DC-DC converter on a custom-designed circuit board and explore time-domain and frequency-domain behavior to reveal insights that mathematical analysis and simulation do not.

III Analytical State Verification

Based on the aforementioned control scheme, 4 distinct states can be derived [3]. These states are S_0 on S_1 on, S_0 on S_1 off, S_0 off S_1 on, and S_0 off S_1 off respectively. The differential expressions for inductor current, v_{o1}, and v_{o2} are derived below.

State A

$$\frac{V_L}{L} = \frac{di_L}{dt} \rightarrow \frac{di_L}{dt} = \frac{Vin - v_{o1}}{L}$$
$$\frac{I_{C1}}{C} = \frac{dv_{o1}}{dt} \rightarrow \frac{dv_{o1}}{dt} = \frac{I_L - \frac{v_{o1}}{R_1}}{C_1}$$
$$\frac{I_{C2}}{C} = \frac{dv_{o2}}{dt} \rightarrow \frac{dv_{o2}}{dt} = \frac{-\frac{v_{o2}}{R_2}}{C_2}$$

State B

$$\frac{V_L}{L} = \frac{di_L}{dt} \rightarrow \frac{Vin - v_{o2}}{L} = \frac{di_L}{dt}$$
$$\frac{I_{C1}}{C} = \frac{dv_{o1}}{dt} \rightarrow \frac{dv_{o1}}{dt} = \frac{-\frac{v_{o1}}{R_1}}{C_1}$$
$$\frac{I_{C2}}{C} = \frac{dv_{o2}}{dt} \rightarrow \frac{dv_{o2}}{dt} = \frac{I_L - \frac{v_{o2}}{R_2}}{C_2}$$

State C

$$\frac{V_L}{L} = \frac{di_L}{dt} \rightarrow \frac{di_L}{dt} = \frac{-v_{o1}}{L}$$
$$\frac{I_{C1}}{C} = \frac{dv_{o1}}{dt} \rightarrow \frac{dv_{o1}}{dt} = \frac{I_L - \frac{v_{o1}}{R_1}}{C_1}$$
$$\frac{I_{C2}}{C} = \frac{dv_{o2}}{dt} \rightarrow \frac{dv_{o2}}{dt} = \frac{-\frac{v_{o2}}{R_2}}{C_2}$$

State D

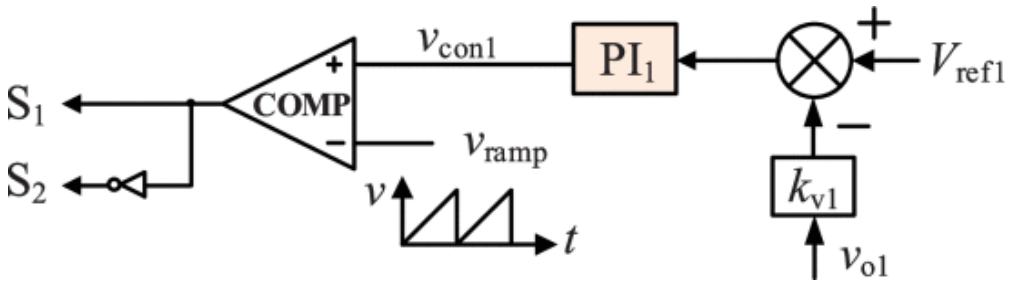
$$\frac{V_L}{L} = \frac{di_L}{dt} \rightarrow \frac{di_L}{dt} = \frac{-v_{o2}}{L}$$
$$\frac{I_{C1}}{C} = \frac{dv_{o1}}{dt} \rightarrow \frac{dv_{o1}}{dt} = \frac{-\frac{v_{o1}}{R_1}}{C_1}$$
$$\frac{I_{C2}}{C} = \frac{dv_{o2}}{dt} \rightarrow \frac{dv_{o2}}{dt} = \frac{I_L - \frac{v_{o2}}{R_2}}{C_2}$$

These analytical results match the analytical results from [1].

IV Control System

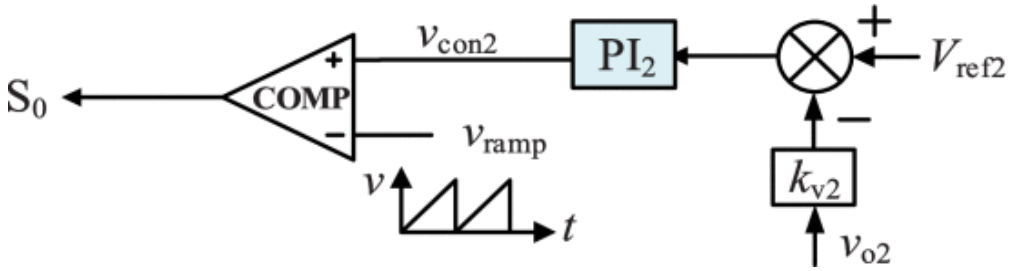
Overview

The control system for this SIDO design consists of 2 control stages. The first stage controls S1 and S2 by reading the voltage across v_{o1} and using it to spread the voltage between the 2 outputs.



Control Stage 1

The second stage controls S_0 by reading the voltage across v_{o2} and using it to regulate the amount of power transferred into the second stage of the system.

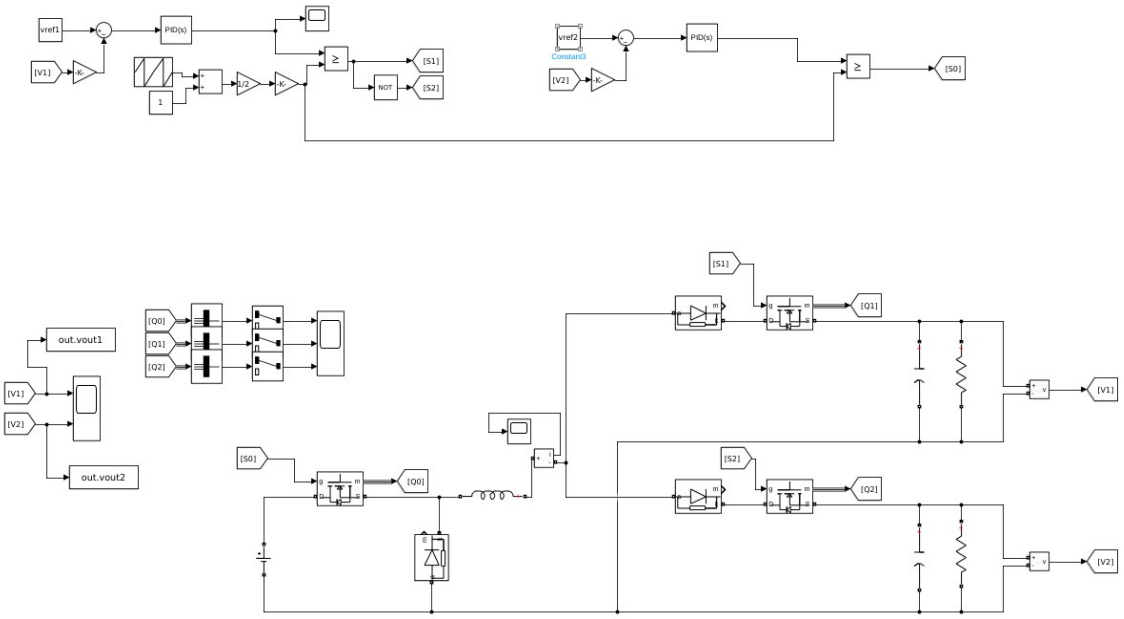


Control Stage 2

Therefore, control stage 1 keeps the power to output 1 constant, which allows the power on output 2 to swing with the input power.

Simulation

In the paper, a spice model was chosen in order to verify the results of the converter control system. Because of the complexities involved with this approach, we chose to utilize a Simulink based approach to model our simulation, as it allows us to verify the papers results using a different approach, as well as allowing us to test more scenarios. Below is an overview of our Simulink model.



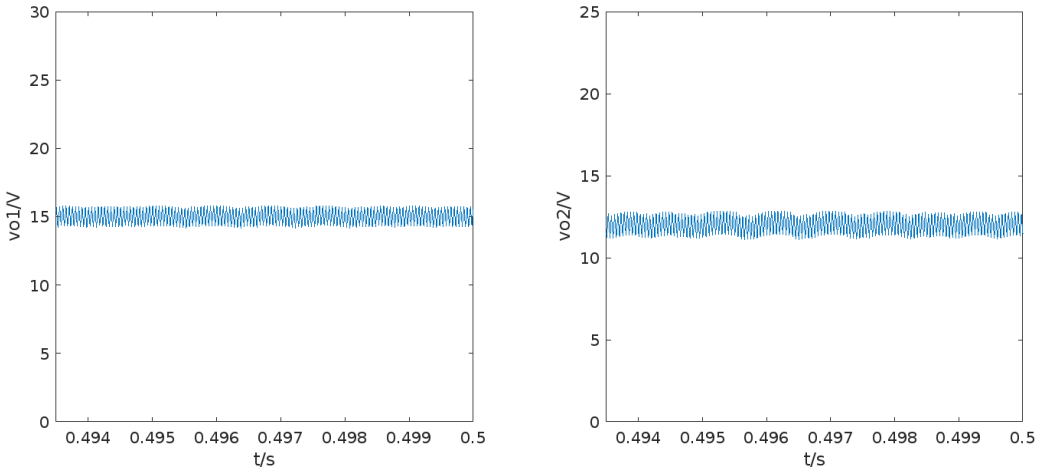
Simulink Model

We first utilized the parameters used in the paper's simulation, and plugged them in as variables to ours, and compared the results. Below are the parameters of the base simulation.

Components/parameters	Values
Input voltage V_{in}	30V
Inductance L	1mH
Capacitance C_1, C_2	47μF,47μF
Voltage sensor gains k_{v1}, k_{v2}	0.1,0.1
Reference voltages V_{ref1}, V_{ref2}	1.5V,1.2V
PI coefficients k_{p1}, T_{p1}, k_{p2}, T_{p2}	0.47,0.0001,1.05,0.001
Switching frequency f_s	20kHz
Amplitude of the ramp V_M	3V

Parameters used in simulation

Note the fact that there is a scalar kv1 and kv2, which are both set to 0.1. This has the effect of dividing the reference voltage by 0.1, so the expected output of vo1 and vo2 are 15V and 12V respectively. Below is the case where both resistors are set to 5 ohms.



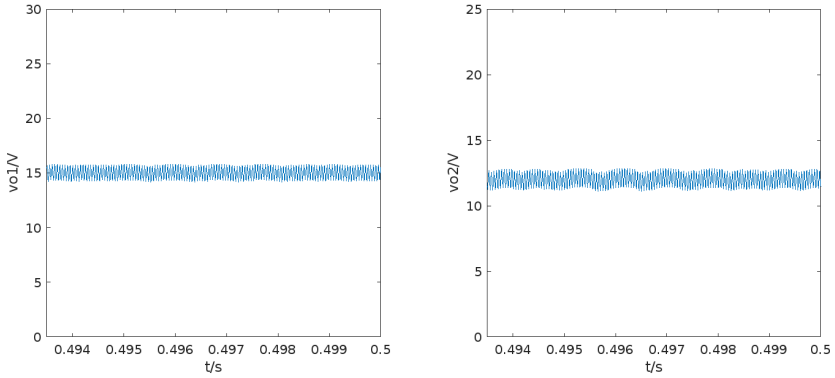
R_1=5Ω, R_2=5Ω, Time-Domain Waveform

This output is in line with the output from the paper, as seen below.

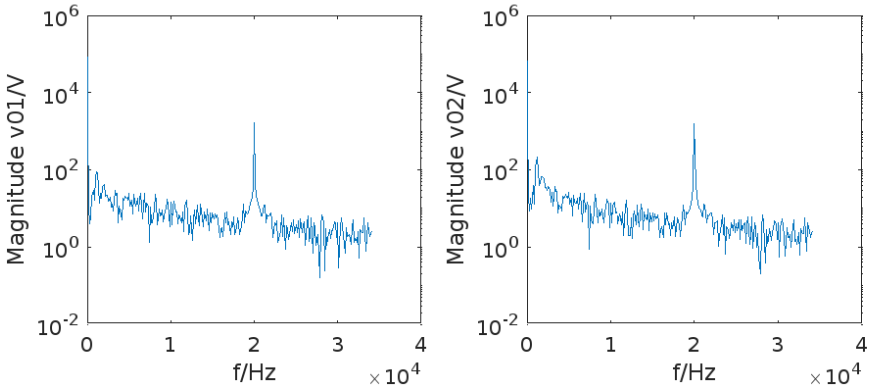
V Simulated Harmonics

Simulation

When looking at the harmonic effects for the outputs of this converter, an interesting phenomenon occurs. When both resistors are set to 5 ohms, the output frequency spectrum is what one would expect, with a DC component and a spike at the switching frequency of 20kHz.

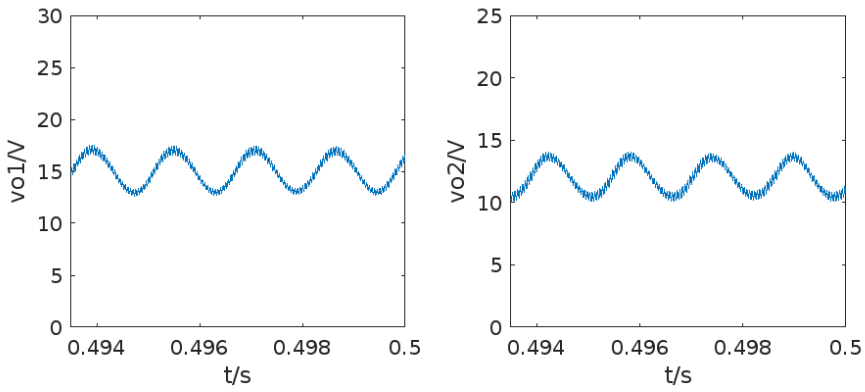


R_1=5Ω R_2=5Ω Time Domain

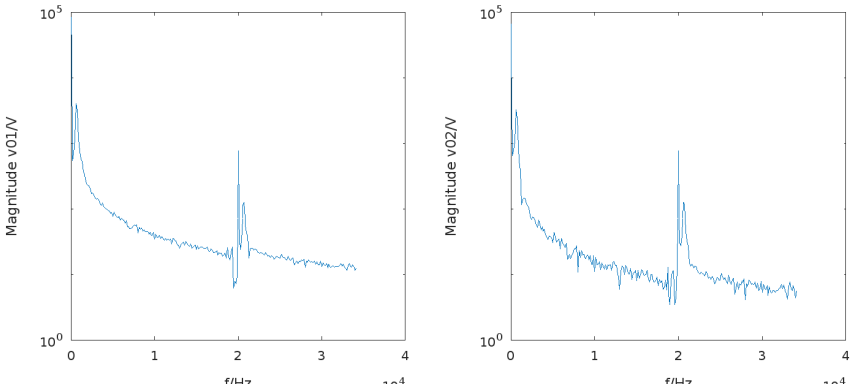


R_1=5Ω R_2=5Ω Frequency Domain

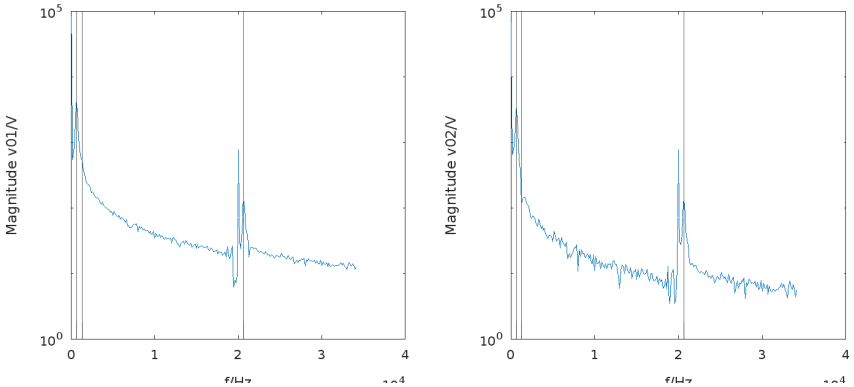
However, when the load resistance for both outputs is raised to 10 ohms, the output waveform develops some harmonics, as seen below. These harmonics occur at fa1=647Hz, fa2=2*fa1=1294Hz, and fa3=fa1+fs=20647Hz.



R_1=10Ω R_2=10Ω Time Domain

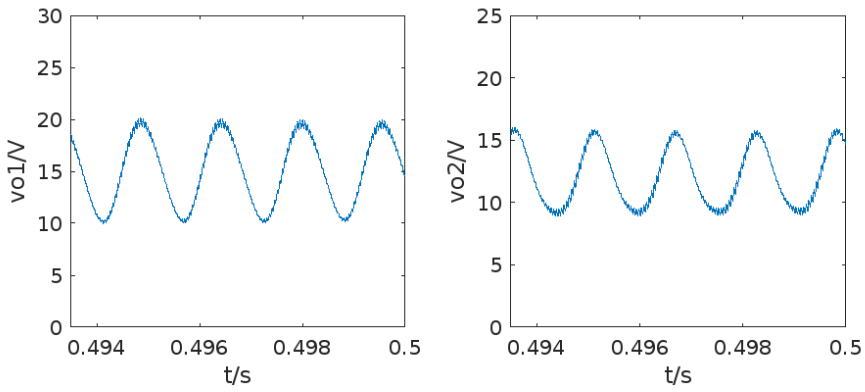


R_1=10Ω R_2=10Ω Frequency Domain

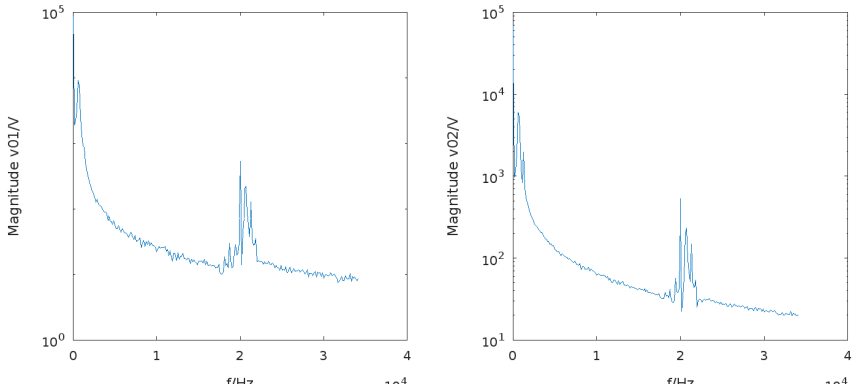


R_1=10Ω R_2=10Ω Frequency Domain

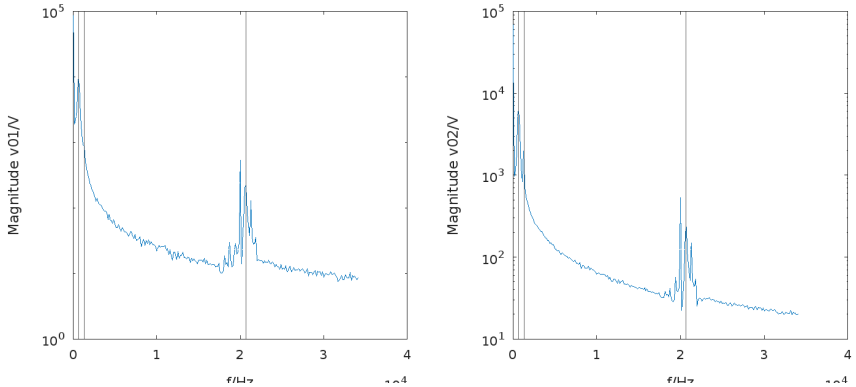
When the resistance is increased to 13 ohms, the distortion of the waveform increases, and the harmonics now appear at 654Hz, 1308Hz, and 20654Hz.



R_1=13Ω R_2=13Ω Time Domain

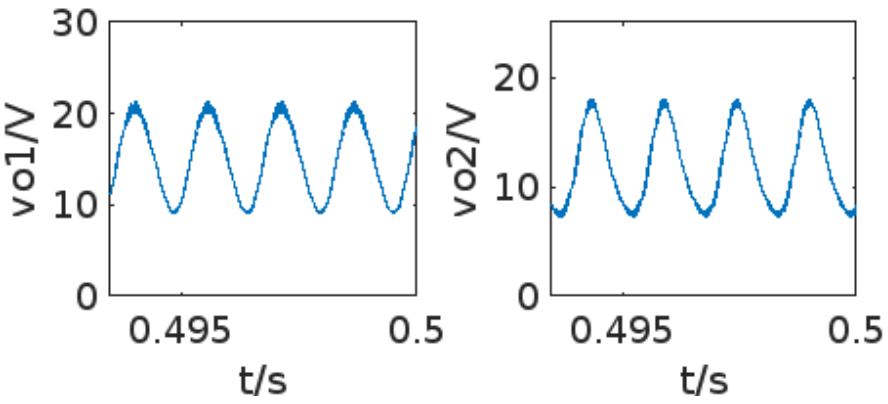


R_1=13Ω R_2=13Ω Frequency Domain

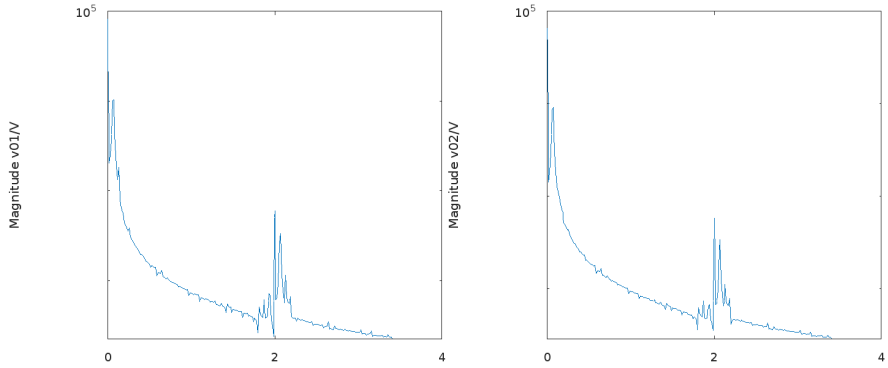


R_1=13Ω R_2=13Ω Frequency Domain

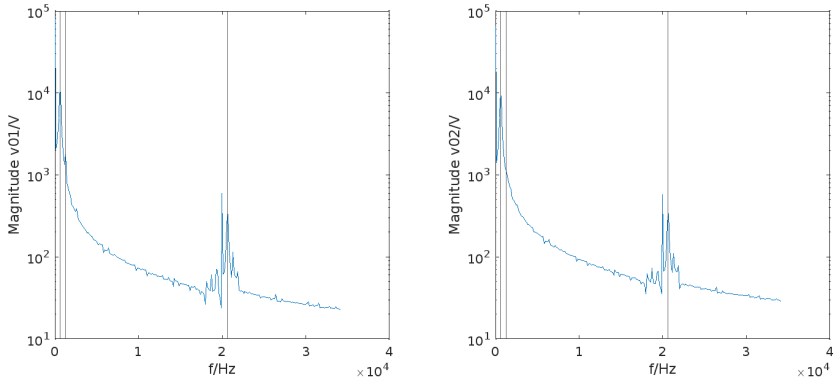
To test this further, R_1 is set to 9 ohms and R_2 10 ohms in order. The harmonics now occur at 648Hz, 1296Hz, and 20648Hz.



R_1=9Ω R_2=10Ω Time Domain



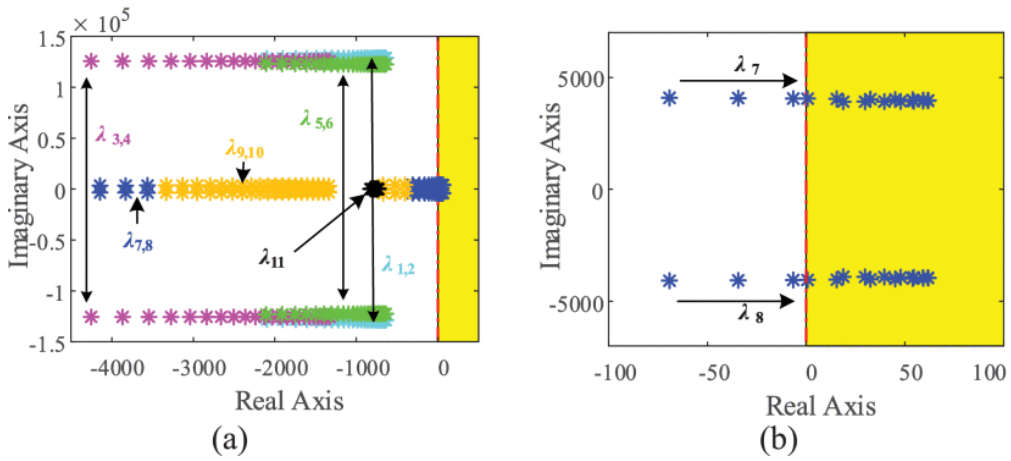
R_1=9Ω R_2=10Ω Time Domain



R_1=9Ω R_2=10Ω Time Domain

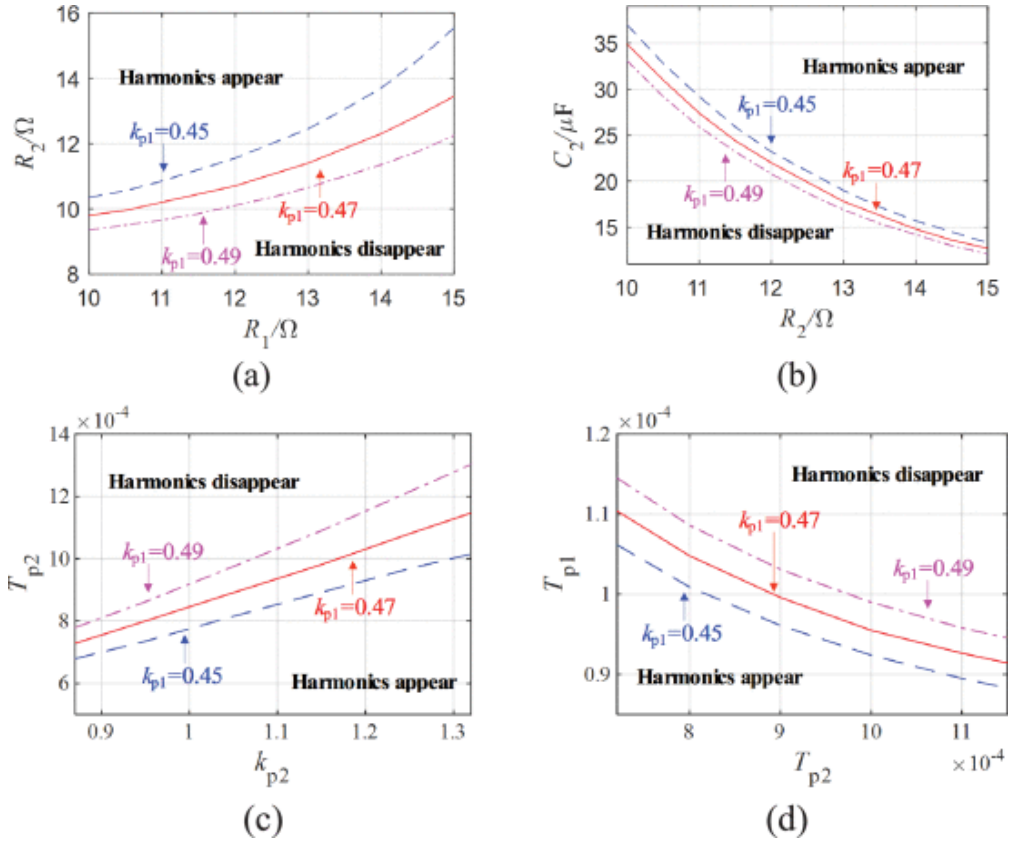
Regions

To investigate this behavior, the paper did an eigenvalue analysis to determine the border between these 2 regions. Using this approach, the paper is able to determine the eigenvalues of the characteristic equation, which correspond to the roots of the control system. The graph below shows the path of these roots as R_1 and R_2 are increased.



Eigenvalue Trajectories

As can be seen, past a certain value, roots 7 and 8 move to the right of the imaginary axis, which correspond to the appearance of harmonics in the system. Below is a diagram developed by the paper showing when eigenvalues appear based on certain variables.



Regions of Harmonica from Eigenvalue Analysis

As can be seen in the top left graph, (5,5) falls below the line, corresponding to no harmonics, whereas (10, 10), (13, 13) and (9, 10) fall above the line, corrosponding to the introduction of harmonics.

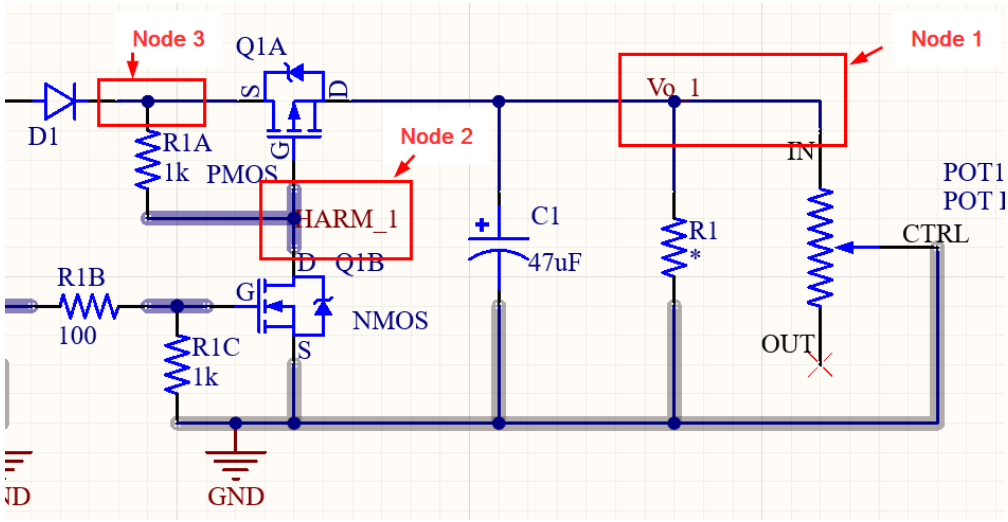
VI Experimental Design

A Experimental Goals

The goal of this experiment was to measure the time-domain waveform and frequency-domain spectrum of different circuit nodes for multiple duty cycles of both switch 0 and switch 1/2.

Specifically, 3 nodes were chosen:

1. **Node 1 - Load Node**
2. **Node 2 - PMOS Gate Node**
3. **Node 3 - PMOS Source Node**



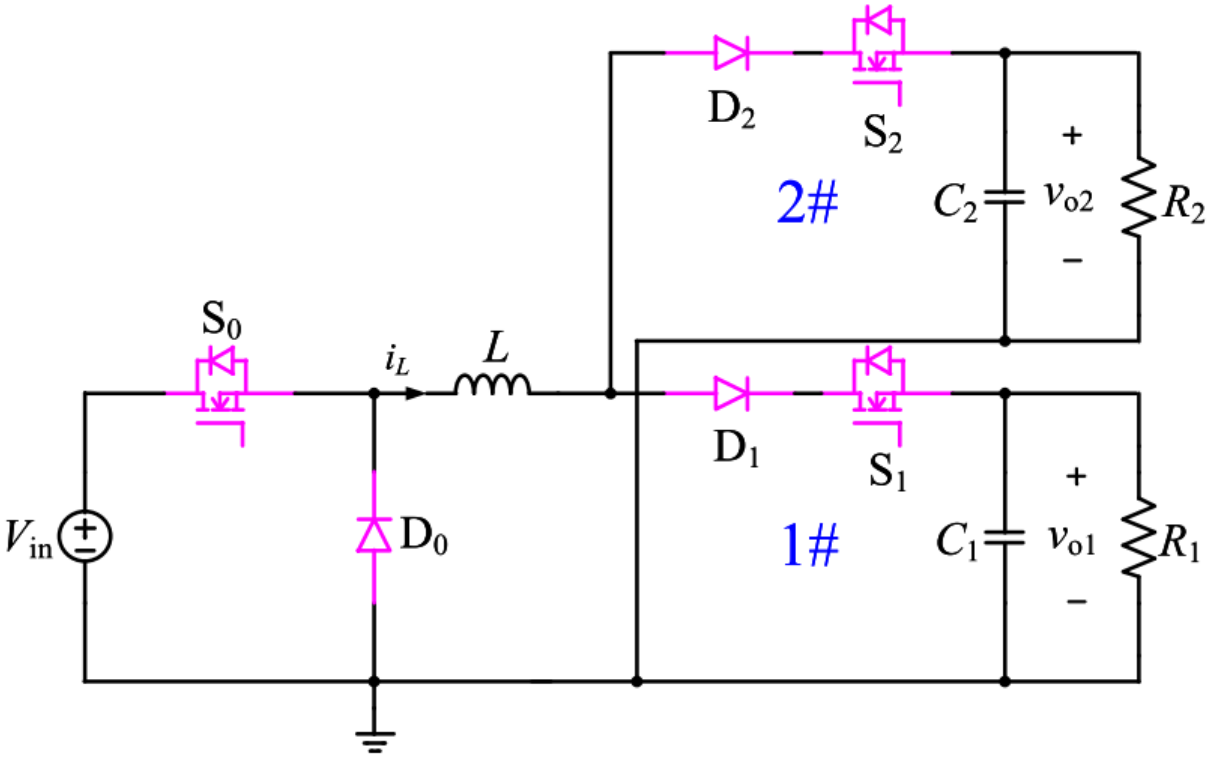
Test Circuit Schematic labeled with test nodes

We chose to record data at subcircuit 1 (i.e. the subcircuit concerned with v_{o1}) and verify that the same behavior was mirrored in subcircuit 2. We seek to explore two questions by performing these tests:

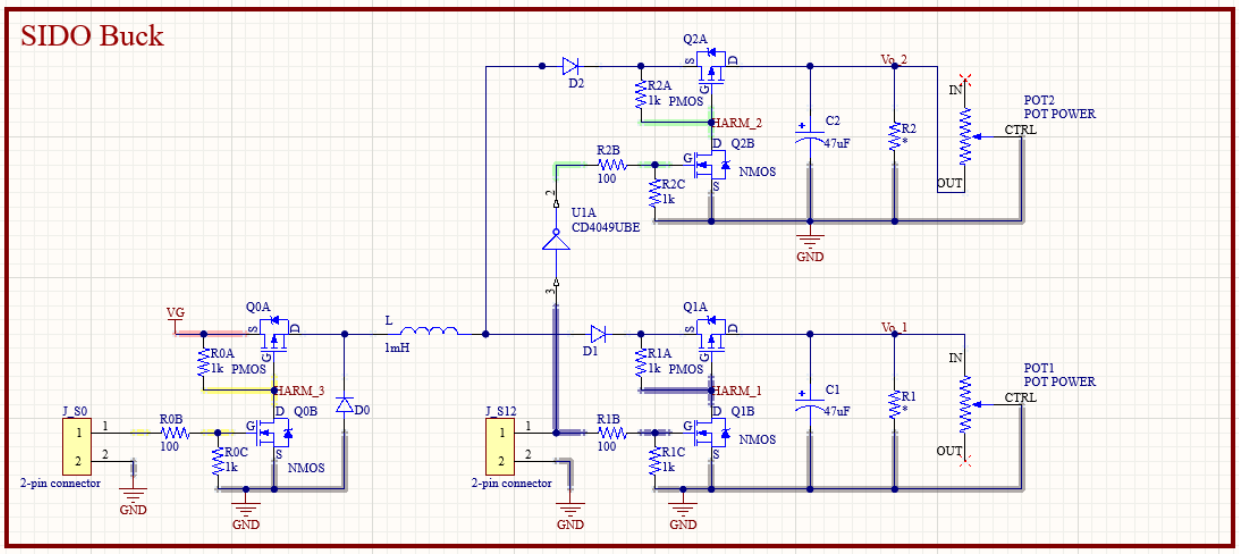
1. **What novel design challenges arise when implementing an abstract mathematical model or computer simulation model in a concrete circuit?**
2. **How might the time-domain waveform and frequency-domain spectrum measurements inform proper component selection?**

B Circuit Board Design and Specification

Our experimental setup consisted of a custom-designed circuit board to mimic [1]'s abstract circuit schematic as closely as possible.

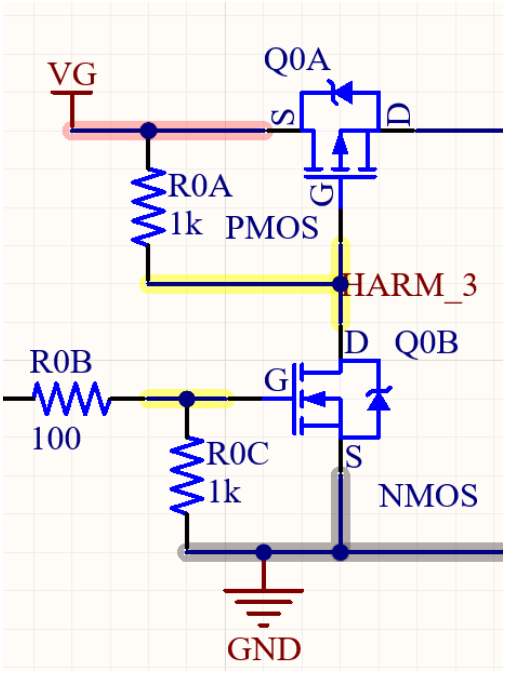


SIDO Buck Converter Schematic Given by [1]



SIDO Buck Converter Schematic for our experimental validation

The paper [1] shows the use of an NMOS as a high-side switching element at multiple points of the circuit. To achieve high-side switching with ground as a low signal voltage reference, the converter's switching functionality was implemented by using an NMOS-controlled-PMOS topology. This allows the use of active-high switching logic on an NMOS that controls a PMOS acting as a high-side switch, making possible the use of low control voltages to drive high source voltages.



Implementation of converter switching circuitry using NMOS-controlled-PMOS

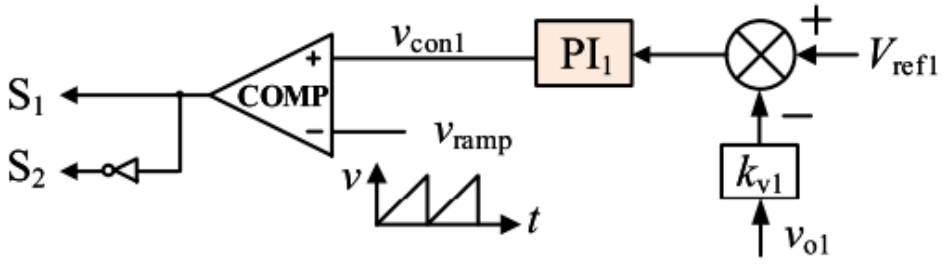
Our design includes pull-up resistors between the PMOS gate and source and pull-down resistors between the NMOS gate and ground to prevent spurious switching.

In addition, the current through a capacitor is given by

$$I_{Gate}(t) = \frac{V_{switch}}{R_{series}} \cdot e^{\frac{-t}{RC}}$$

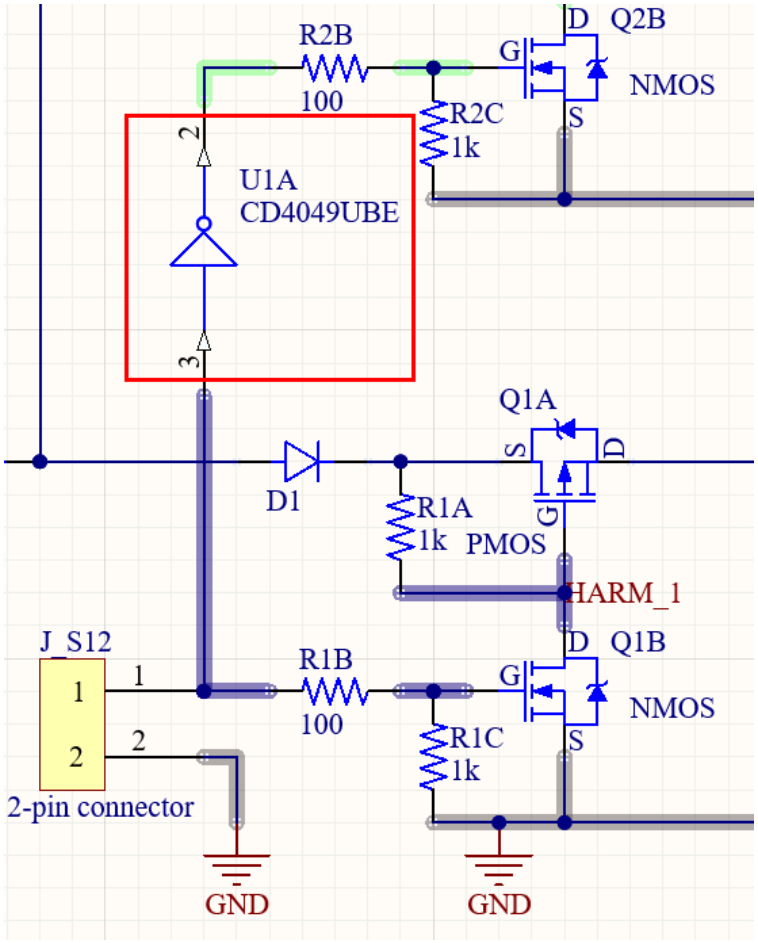
Without an included discrete series resistance, the FET gate's capacitance may have a very low equivalent series resistance. Therefore, a series resistor on the gate of the NMOS limits large current draw at the onset of a fast-rising edge through the MOSFET's gate capacitance.

The paper [1] specifies a complimentary switching period control scheme for S1 and S2, as specified by the below control system diagram:



Complimentary switching period control scheme for S1 and S2

Therefore, our test circuit includes an inverter to invert the control signal applied to S1:

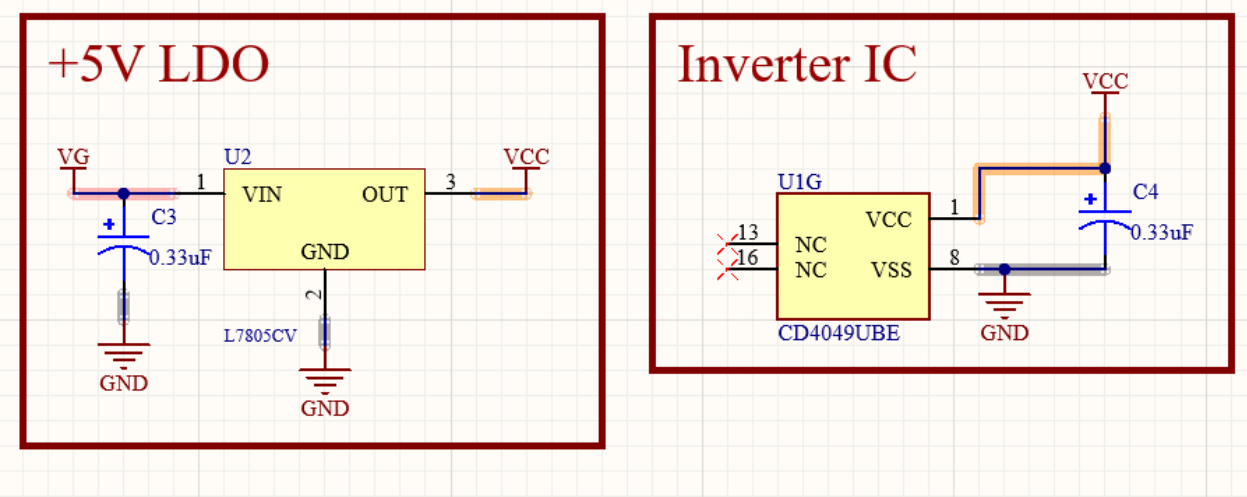


Inverter between S1 and S2 control signals

The component values and product numbers included in our test circuit are as follows:

Component Designator	Component Value	Component Product Number
C_1, C_2	$47\mu F$	UCS2E470MHD1TO
D_0, D_1, D_2	$V_F = 650mV@5A$	SB560-E3/54
J_{S0}, J_{S12}	-	SB560-E3/54
L	$1mH, R_{series} = 0.4\Omega$	2124-H-RC
POT_1, POT_2	5Ω	026TB32R5A0B1A1
Q_{0A}, Q_{1A}, Q_{2A}	PMOS	FQPF9P25
Q_{0B}, Q_{1B}, Q_{2B}	NMOS	FDP090N10
$R_{0A}, R_{0C}, R_{1A}, R_{1C}, R_{2A}, R_{2C}$	$1k\Omega$	HRG3216P-1001-D-T1
R_{0B}, R_{1B}, R_{2B}	100Ω	CRCW1206100RFKEAHP
R_1, R_2	Not placed	-
All test points	-	RCWCTE
U_1	Inverter IC	CD4049UBE

Our test circuit also includes a LDO regulator and decoupling capacitor to power the inverter IC:



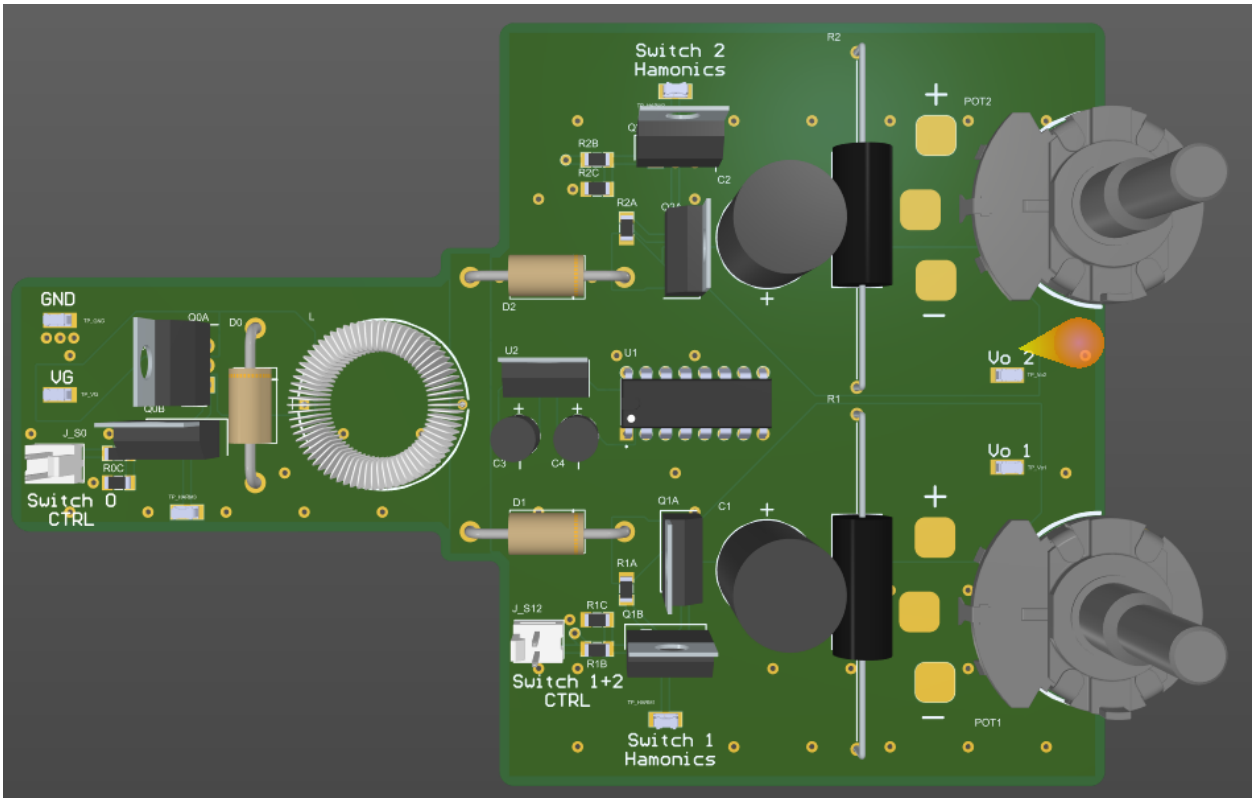
Linear regulator for inverter IC

Component Designator	Component Value	Component Product Number
C_3, C_4	$0.33\mu F$	UVR2AR33MDD1TD
U_2	Linear Regulator	L7805CV

The test conditions applied to the circuit were as follows for all test cases:

Parameter	Value
Input voltage V_g	$15V$
Switching frequency f_s	$20kHz$
$S_{0,1,2}$ LOW voltage	$0V$
$S_{0,1,2}$ HIGH voltage	$5V$

The final PCB render looks as such:



SIDO Buck Converter Test PCB

The following test equipment was used:

Equipment	Manufacturer	Manufacturer Product Number
DC Power Supply	RIGOL	DP831A
Signal Generator	RIGOL	DG1022
Digital Multimeter	RIGOL	DM3058
Digital Oscilloscope	RIGOL	DS1102
Spectrum Analyzer	RIGOL	DS8600

C Test procedure

Using the previously defined component values and test conditions, the test procedure was as follows:

1. Connect $+15V$ and GND to the respective test points V_g and GND on the PCB.
2. Connect oscilloscope and spectrum analyzer probes to the load node.
   (a) Apply a square wave control signal with a 50% duty cycle to Switch 0.
   (b) Apply a square wave control signal with an 80% duty cycle to Switch 1.
   (c) Capture the oscilloscope and spectrum analyzer outputs.
   (d) Repeat steps b-c for duty cycles of $85\%, 90\%, 95\%$, and 99% on Switch 1.
   (e) Repeat steps a-d for duty cycles of $60\%, 70\%$, and 80% on Switch 0.
3. Repeat step 2 at the PMOS gate node and the PMOS source node.

In total, we captured:

$$\begin{gathered}\text{5 Switch 1 duty cycles} \\ \times \text{4 Switch 0 duty cycles} \\ \times \text{2 Test equipment output images per measurement} \\ \times \text{3 Circuit Nodes} \\ \boxed{= \text{120 Test equipment output images}}\end{gathered}$$

VII Experimental Results - Images

Our experimental results are contained in Appendices A-C. The legend for the results are as follows:

Figure X(a): Oscilloscope Image of Test Conditions in question
Figure X(b): Spectrum Analyzer Image of Test Conditions in question

Appendix A - Load Node Measurements

Contains Figures 1-20, which are the results of measuring the voltage at the load node for all combinations of $S_0 = 50\%, 60\%, 70\%, 80\%$ duty cycle and $S_1 = 80\%, 85\%, 90\%, 95\%, 99\%$ duty cycle.

Appendix B - PMOS Gate Node Measurements

Contains Figures 21-40, which are the results of measuring the voltage at the PMOS gate node for all combinations of $S_0 = 50\%, 60\%, 70\%, 80\%$ duty cycle and $S_1 = 80\%, 85\%, 90\%, 95\%, 99\%$ duty cycle.

Appendix C PMOS Source Node Measurements

Contains Figures 41-60, which are the results of measuring the voltage at the PMOS source node for all combinations of $S_0 = 50\%, 60\%, 70\%, 80\%$ duty cycle and $S_1 = 80\%, 85\%, 90\%, 95\%, 99\%$ duty cycle.

VIII Experimental Results - Discussion

A Transients

Very large voltage spikes can be seen in many of the time-domain waveforms captured by the oscilloscope. These spikes are concentrated at the PMOS gate and source nodes, and peak in our measurements when S_1 is driven with an 80% duty cycle and S_0 is driven with a 50% duty cycle. We see the peaks of these transients decrease as the switch 1 duty cycle is increased.

Specifically, figure 21(a) shows transient voltage spikes and the PMOS gate node peaking at approximately 55V. Figure 41(a) shows the transient voltage spikes and the PMOS source node peaking at approximately 43.6V.

These sharp spikes occur at the moment that the NMOS switches off. The voltage across an inductor is given by:

$$V_L = L\frac{di}{dt}$$

As current cannot instantaneously change in an inductor, these voltage transients should be expected during periods of fast switching where the inductor resists rapid changes in current via increases in voltage, which appear here at the PMOS gate and source nodes.

These transients do not occur in our abstract circuit analysis because we assume ideal state transitions between switches 1 and 2. We seem to be observing latency between the complimentary switching of switch 1 and switch 2, which might be attributed to the selected inverter, CD4049UBE, which is shown to have a maximum latency of 120ns. It may also arise from die mismatch of the discrete transistors used in subcircuits 1 and 2.

If this SIDO buck converter topology is to be utilized effectively, components must be selected to withstand both the steady state voltage, current, and power conditions and the transient voltage and current spikes. Furthermore, switching elements that are matched in the same silicon die and a low-latency inverter might decrease switching transient severity, as will using high switching duty cycles to decrease the peak transient value.

B Harmonics

Harmonics that result from highly non-linear time-domain waveforms were observed in the spectrum of the PMOS gate and source nodes. One expects harmonics on these nodes

resulting from the Fourier representation of the square wave control signal given by

$$f(x) = \frac{A}{2} + \frac{2A}{\pi}(\sum_{n=1,3,5,...} \frac{1}{n} sin(n \cdot \omega_0 t))$$

While we do see integer multiple harmonics that are evenly spaced on the spectrum, we see spectral components at all integer multiple frequencies of the fundamental, not just odd integer multiples.

We also do not see constant $\frac{1}{n}$ scaling of the amplitudes of the harmonic spikes. For example, Figure 21(b) shows harmonics at integer multiple frequencies, but with an amplitude pattern closer to that of $|\frac{sin(x)}{x}|$.

If this SIDO buck converter topology is to be utilized effectively, this harmonic content must be taken into account when analyzing efficiencies. Specifically, if high switching frequencies are used, care must be taken to select switching elements that will minimize harmonic losses.

IX Conclusion

In this paper, the mathematical analysis, SIMULINK simulation, and concrete circuit implementation have been applied to a SIDO buck converter topology defined by [1]. The mathematical analysis verifies that of [1] and the novel simulation has been used to produce another expression of the results found in [1]. Furthermore, the SIDO buck converter PCB experiments have revealed more insight into the challenges of practical implementation of this particular topology.

Multiple-output DC-DC converter topologies may be required in applications to maximize efficiency through integrated systems. However, due to the effects of harmonic resonance between the two outputs, transient voltage spikes resulting from non-ideal switching conditions, and the complexity of their control system, the SIDO buck converter topology analyzed in this paper introduces many novel design challenges that must be accounted for. They may be able to save space and cost on inductors for high-current applications; however, similar to the DCM mode in traditional converters, one must also avoid the resonance region of these converters in order for them to be practical and size components to properly handle transient conditions.

X References

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